VIDYAVARDHAKA COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Time Table for Academic Year 2020-21 ODD Semester

Semester: III **Section: 'A'** **Room No. :**

TIME / DAY	8.15-8.55	9.00-9.40	9.45-10.25	10.25 - 11.00	11.00-11.40	11.45-12.25	12.30-2.00	2.00-2.40	2.45-3.25	3.30-4.10
MON		18MAT31 (RBR)	18EC35 (SM)	**TEA BREAK**	18ECL37 (AVD+VKS)- A1		**LUNCH BREAK**			
					18ECL38 (SK+JSS)- A2					
TUE		18EC35 (SM)	18MAT31 (RBR)		18ECL37 (AVD+VKS)- A2					
					18ECL38 (SK+PSV)- A3					
WED		18EC36 (JB)	18EC32 (APK)		18MAT31 (RBR)	18EC33 (AVD)		18ECL37 (AVD+VKS)- A3		
								18ECL38 (SK+PSV)- A1		
THU		18EC32 (APK)	18EC34 (GA)		18EC36 (JB)	18MAT31 (RBR)		18EC32 (APK)	18CPC39	
FRI	18MAT31 (RBR)	18EC33 (AVD)	18EC36 (JB)		18EC32 (APK)	18EC34 (GA)				
SAT		18EC34 (GA)	18EC33 (AVD)		18EC35 (SM)	18EC32 (APK)				

Subject Code	Subject Name	Faculty Name
18MAT31	Mathematics	Dr. Rakshith B R (RBR)
18EC32	Network Theory	MS. Kavya A P (APK)
18EC33	Electronic Devices	Mr. Alfred Vivek D'Souza (AVD)
18EC34	Digital System Design	Dr. Geethashree A (GA)
18EC35	Computer Organization & Architecture	Dr. Suchitra M (SM)
18EC36	Power Electronics & Instrumentation	Mr. Jagadeesh B (JB)
18ECL37	Electronic Devices & Instrumentation Lab	
18ECL38	Digital System Design Lab	
18CPC39	Constitution of India, Professional Ethics and Cyber Law	

VIDYAVARDHAKA COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Time Table for Academic Year 2020-21 ODD Semester

Semester: III **Section: 'B'** **Room No. :**

TIME / DAY	8.15-8.55	9.00-9.40	9.45-10.25	10.25 - 11.00	11.00-11.40	11.45-12.25	12.30-2.00	2.00-2.40	2.45-3.25	3.30-4.10
MON		18MAT31 (MKJ)	18EC33 (BHS)	**TEA BREAK**	18EC36 (CK)	18EC34 (SKV)	**LUNCH BREAK**	18CPC39	18EC32 (KB)	
TUE		18EC36 (CK)	18EC34 (SKV)		18EC35 (SR)	18MAT31 (MKJ)				
WED		18EC35 (SR)	18MAT31 (MKJ)		18ECL37 (APK+BK)- B2					
					18ECL38 (TS+K)- B3					
THU		18EC34 (SKV)	18EC32 (KB)		18ECL37 (APK+BK)- B3					
					18ECL38 (SKV+K)- B1					
FRI		18EC33 (BHS)	18EC35 (SR)		18MAT31 (MKJ)	18EC32 (KB)		18ECL37 (APK+BK)- B1		
								18ECL38 (SKV+K)- B2		
SAT	18MAT31 (MKJ)	18EC32 (KB)	18EC36 (CK)		18EC33 (BHS)	18EC32 (KB)				

Subject Code	Subject Name	Faculty Name
18MAT31	Mathematics	Dr. Manasa K J (MKJ)
18EC32	Network Theory	Mrs. Kavyashree B (KB)
18EC33	Electronic Devices	Mrs. Bhanu H S (BHS)
18EC34	Digital System Design	Mr. Sudheesh K V (SKV)
18EC35	Computer Organization & Architecture	Dr. Shilpa R (SR)
18EC36	Power Electronics & Instrumentation	Mr. Chethan K (CK)
18ECL37	Electronic Devices & Instrumentation Lab	
18ECL38	Digital System Design Lab	
18CPC39	Constitution of India, Professional Ethics and Cyber Law	

VIDYAVARDHAKA COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Time Table for Academic Year 2020-21 ODD Semester

Semester: III **Section: 'C'** **Room No. :**

TIME / DAY	8.15-8.55	9.00-9.40	9.45-10.25	10.25 - 11.00	11.00-11.40	11.45-12.25	12.30-2.00	2.00-2.40	2.45-3.25	3.30-4.10
MON		18EC34 (AAA)	18EC33 (GRK)	**TEA BREAK**	18MAT31 (PKN)	18EC36 (KKH)	**LUNCH BREAK**	18EC32 (BK)	18CPC39	
TUE		18EC36 (KKH)	18MAT31 (PKN)		18EC34 (AAA)	18EC32 (BK)				
WED		18MAT31 (PKN)	18EC34 (AAA)		18EC33 (GRK)	18EC35 (TS)				
THU		18EC32 (BK)	18EC36 (KKH)		18EC35 (TS)	18MAT31 (PKN)		18ECL37 (AVD+GRK)- C1		
								18ECL38 (AAA+JSS)- C2		
FRI		18EC35 (TS)	18EC32 (BK)		18ECL37 (AVD+GRK)- C2					
					18ECL38 (AAA+JSS)- C3					
SAT	18MAT31 (PKN)	18EC33 (GRK)	18EC32 (BK)		18ECL37 (CDJ+GRK)- C3					
					18ECL38 (AAA+TS)- C1					

Subject Code	Subject Name	Faculty Name
18MAT31	Mathematics	Mr. Prakasha K N (PKN)
18EC32	Network Theory	Mrs. Bhargavi K (BK)
18EC33	Electronic Devices	Mr. Ravikrishna G (RG)
18EC34	Digital System Design	Ms. Audre Arlene A (AAA)
18EC35	Computer Organization & Architecture	Mrs. Tejaswini S (TS)
18EC36	Power Electronics & Instrumentation	Mr. Kirankumar Humse (KKH)
18ECL37	Electronic Devices & Instrumentation Lab	
18ECL38	Digital System Design Lab	
18CPC39	Constitution of India, Professional Ethics and Cyber Law	

VIDYAVARDHAKA COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Time Table for Academic Year 2020-21 ODD Semester

Semester: III **Section: 'D'** **Room No. :**

TIME / DAY	8.15-8.55	9.00-9.40	9.45-10.25	10.25 - 11.00	11.00-11.40	11.45-12.25	12.30-2.00	2.00-2.40	2.45-3.25	3.30-4.10
MON		18EC33 (CDJ)	18MAT31 (RBR)	**TEA BREAK**	18EC34 (PSV)	18EC35 (JV)	**LUNCH BREAK**	DIPMAT		
TUE	18MAT31 (RBR)	18EC35 (JV)	18EC36 (RB)		18EC32 (JSS)	18EC33 (CDJ)		18ECL37 (CDJ+TS)- D1		
WED		18EC32 (JSS)	18EC34 (PSV)		18EC32 (JSS)	18MAT31 (RBR)		DIPMAT		
THU		18EC36 (RB)	18EC35 (JV)		18MAT31 (RBR)	18EC34 (PSV)		18CPC39		
FRI		18MAT31 (RBR)	18EC32 (JSS)		18EC36 (RB)	DIPMAT				
SAT	18ECL38 (SK+PSV)- D1				18EC33 (CDJ)	18EC32 (JSS)				

Subject Code	Subject Name	Faculty Name
18MAT31	Mathematics	Dr. Rakshith B R (RBR)
18EC32	Network Theory	Mr. Jayanna S S (JSS)
18EC33	Electronic Devices	Ms. Chaithanya D J (CDJ)
18EC34	Digital System Design	Ms. Panchami S V (PSV)
18EC35	Computer Organization & Architecture	Mr. Jashwanth V (JV)
18EC36	Power Electronics & Instrumentation	Ms. Ramya B (RB)
18ECL37	Electronic Devices & Instrumentation Lab	
18ECL38	Digital System Design Lab	
18CPC39	Constitution of India, Professional Ethics and Cyber Law	

VIDYAVARDHAKA COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Time Table for Academic Year 2020-21 ODD Semester

Semester: V **Section: 'A'** **Room No. :**

TIME / DAY	8.15-8.55	9.00-9.40	9.45-10.25	10.25 - 11.00	11.00-11.40	11.45-12.25	12.30 -2.00	2.00-2.40	2.45-3.25	3.30-4.10
MON		18EC55 (SNR)	18EC52 (CMP)	**TEA BREAK**	18ECL57 (CMP+SNR+AAP)-A1		**LUNCH BREAK**			
					18ECL58 (SM+JB)-A2					
TUE		18EC53 (VMP)	18EC52 (CMP)		18ECL57 (CMP+SNR+RB)-A2					
					18ECL58 (SM+JB)-A3					
WED		18ES51 (SMS)	18EC56 (SM)		18EC54 (DJR)	18EC53 (VMP)		18ECL57 (CMP+MS+AAP)-A3		
								18ECL58 (GMN+KKH)-A1		
THU		18EC56 (SM)	18EC53 (VMP)		18EC52 (CMP)	18EC55 (SNR)				
FRI		18ES51 (SMS)	18EC54 (DJR)		18EC55 (SNR)	18EC52 (CMP)		18EC53 (VMP)	18EC56 (SM)	18CIV59
SAT		18EC54 (DJR)	18EC52 (CMP)		18EC53 (VMP)	18ES51 (SMS)				

Subject Code	Subject Name	Faculty Name
18ES51	Technological Innovation Management and Entrepreneurship	Ms. Sahana M S (SMS)
18EC52	Digital Signal Processing	Dr. C M Patil (CMP)
18EC53	Principles of Communication Systems	Dr. Vasudha M P (VMP)
18EC54	Information Theory and Coding	Dr. D J Ravi (DJR)
18EC55	Electromagnetic Waves	Dr. Sandeep R (SNR)
18EC56	Verilog HDL	Dr. Suchitra M (SM)
18ECL57	Digital Signal Processing Lab	
18ECL58	HDL Lab	
18CIV59	Environmental Studies	

VIDYAVARDHAKA COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Time Table for Academic Year 2020-21 ODD Semester

Semester: V **Section: 'B'** **Room No. :**

TIME / DAY	8.15-8.55	9.00-9.40	9.45-10.25	10.25 - 11.00	11.00-11.40	11.45-12.25	12.30-2.00	2.00-2.40	2.45-3.25	3.30-4.10
MON		18EC56 (GMN)	18EC52 (SR)	**TEA BREAK**	18EC55 (APK)	18ES51 (PSV)	**LUNCH BREAK**	18EC52 (SR)	18EC53 (RK)	18CIV59
TUE		18EC52 (SR)	18EC54 (DJR)		18EC53 (RK)	18EC56 (GMN)				
WED		18EC54 (DJR)	18EC53 (RK)		18ECL57 (SR+SMS)-B1					
					18ECL58 (GMN+BHS)-B2					
THU		18ES51 (PSV)	18EC53 (RK)		18ECL57 (SR+SMS+AAP)-B2					
					18ECL58 (GMN+KKH)-B3					
FRI		18EC55 (APK)	18EC56 (GMN)		18ES51 (PSV)	18EC52 (SR)		18ECL57 (SMS+RB)-B3		
								18ECL58 (GMN+KKH)-B1		
SAT		18EC53 (RK)	18EC55 (APK)		18EC52 (SR)	18EC54 (DJR)				

Subject Code	Subject Name	Faculty Name
18ES51	Technological Innovation Management and Entrepreneurship	Ms. Panchami S V (PSV)
18EC52	Digital Signal Processing	Dr. Shilpa R (SR)
18EC53	Principles of Communication Systems	Mr. Rohith K (RK)
18EC54	Information Theory and Coding	Dr. D J Ravi (DJR)
18EC55	Electromagnetic Waves	Ms. Kavya A P (APK)
18EC56	Verilog HDL	Mrs. Geetha M N (GMN)
18ECL57	Digital Signal Processing Lab	
18ECL58	HDL Lab	
18CIV59	Environmental Studies	

VIDYAVARDHAKA COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Time Table for Academic Year 2020-21 ODD Semester

Semester: V **Section: 'C'** **Room No. :**

TIME / DAY	8.15-8.55	9.00-9.40	9.45-10.25	10.25 - 11.00	11.00-11.40	11.45-12.25	12.30-2.00	2.00-2.40	2.45-3.25	3.30-4.10
MON		18EC56 (CK)	18ES51 (TS)	**TEA BREAK**	18EC54 (BK)	18EC55 (YJ)	**LUNCH BREAK**	18ECL57 (MS+RB)-C3		
								18ECL58 (CK+BHS)-C1		
TUE		18EC52 (MS)	18EC54 (BK)		18EC53 (VKS)	18ES51 (TS)				
WED		18EC54 (BK)	18EC52 (MS)		18EC53 (VKS)	18EC56 (CK)				
THU		18EC53 (VKS)	18EC55 (YJ)		18EC52 (MS)	18EC56 (CK)		18EC53 (VKS)	18EC52 (MS)	18CIV59
FRI		18EC55 (YJ)	18EC52 (MS)		18ECL57 (MS+AAP)-C1					
					18ECL58 (CK+CDJ)-C2					
SAT		18ES51 (TS)	18EC53 (VKS)		18ECL57 (MS+AAP)-C2					
					18ECL58 (CK+BHS)-C3					

Subject Code	Subject Name	Faculty Name
18ES51	Technological Innovation Management and Entrepreneurship	Mrs. Tejaswini S (TS)
18EC52	Digital Signal Processing	Mr. Mahadevaswamy (MS)
18EC53	Principles of Communication Systems	Mr. Vishwas K Singh (VKS)
18EC54	Information Theory and Coding	Mrs. Bhargavi K (BK)
18EC55	Electromagnetic Waves	Mr. Yashwanth J (YJ)
18EC56	Verilog HDL	Mr. Chethan K (CK)
18ECL57	Digital Signal Processing Lab	
18ECL58	HDL Lab	
18CIV59	Environmental Studies	

VIDYAVARDHAKA COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Time Table for Academic Year 2020-21 ODD Semester

Semester: VII **Section: 'A'** **Room No. :**

TIME / DAY	8.15-8.55	9.00-9.40	9.45-10.25	10.25 - 11.00	11.00-11.40	11.45-12.25	12.30-2.00	2.00-2.40	2.45-3.25	3.30-4.10
MON		17EC74X	17EC73 (KKH)	**TEA BREAK**	17EC72 (K)	17EC75X	**LUNCH BREAK**	17ECL76 (KB+VMP)-A1		
								17ECL77 (GA+PSK)-A2		
TUE		17EC72 (K)	17EC74X		17ECL76 (KB+YJ)-A2					
					17ECL77 (GA+JV)-A1					
WED		17EC73 (KKH)	17EC75X		17EC71 (SK)	17EC73 (KKH)				
THU		17EC71 (SK)	17EC72 (K)		17EC74X	17EC71 (SK)				
FRI		17EC75X	17EC71 (SK)		17EC73 (KKH)	17EC72 (K)				
SAT										

Subject Code	Subject Name	Faculty Name
17EC71	Microwave and Antennas	Mr. Sharath Kumar A J (SK)
17EC72	Digital Image Processing	Mr. Kiran (K)
17EC73	Power Electronics	Mr. Kirankumar Humse (KKH)
17EC741	Multimedia Communication	Mr. Yashwanth J (YJ)
17EC742	Biomedical Signal Processing	Dr. T P Surekha (TPS)
17EC744	Cryptography	Mr. Vishwas K Singh (VKS)
17EC745	CAD for VLSI	Dr. Geethashree A (GA)
17EC752	IOT and Wireless Sensor Networks	Dr. Vasudha M P (VMP)
17EC755	Satellite Communication	Mrs. Kavyashree B (KB), Ms. Ramya B (RB)
17ECL76	Advanced Communication Lab	
17ECL77	VLSI Lab	
17ECP78	Project Work Phase-I + Project Work Seminar	

VIDYAVARDHAKA COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Time Table for Academic Year 2020-21 ODD Semester

Semester: VII **Section: 'B'** **Room No. :**

TIME / DAY	8.15-8.55	9.00-9.40	9.45-10.25	10.25 - 11.00	11.00-11.40	11.45-12.25	12.30-2.00	2.00-2.40	2.45-3.25	3.30-4.10
MON		17EC74X	17EC71 (RK)	**TEA BREAK**	17EC73 (GRK)	17EC75X	**LUNCH BREAK**			
TUE		17EC71 (RK)	17EC74X		17EC72 (AAP)	17EC73 (GRK)		17ECL76 (RK+YJ)-B1		
								17ECL77 (PSK+BHS)-B2		
WED		17EC73 (GRK)	17EC75X		17ECL76 (RK+YJ)-B2					
					17ECL77 (PSK+JV)-B1					
THU		17EC72 (AAP)	17EC73 (GRK)		17EC74X	17EC71 (RK)				
FRI		17EC75X	17EC72 (AAP)		17EC71 (RK)	17EC72 (AAP)				
SAT										

Subject Code	Subject Name	Faculty Name
17EC71	Microwave and Antennas	Mr. Rohith K (RK)
17EC72	Digital Image Processing	Ms. Aisiri A P (AAP)
17EC73	Power Electronics	Mr. Ravikrishna G (RG)
17EC741	Multimedia Communication	Mr. Yashwanth J (YJ)
17EC742	Biomedical Signal Processing	Dr. T P Surekha (TPS)
17EC744	Cryptography	Mr. Vishwas K Singh (VKS)
17EC745	CAD for VLSI	Dr. Geethashree A (GA)
17EC752	IOT and Wireless Sensor Networks	Dr. Vasudha M P (VMP)
17EC755	Satellite Communication	Mrs. Kavyashree B (KB), Ms. Ramya B (RB)
17ECL76	Advanced Communication Lab	
17ECL77	VLSI Lab	
17ECP78	Project Work Phase-I + Project Work Seminar	

VIDYAVARDHAKA COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Time Table for Academic Year 2020-21 ODD Semester

Semester: VII **Section: 'C'** **Room No. :**

TIME / DAY	8.15-8.55	9.00-9.40	9.45-10.25	10.25 - 11.00	11.00-11.40	11.45-12.25	12.30-2.00	2.00-2.40	2.45-3.25	3.30-4.10
MON		17EC74X	17EC72 (JV)	**TEA BREAK**	17EC73 (CDJ)	17EC75X	**LUNCH BREAK**			
TUE		17EC71 (PSK)	17EC74X		17EC72 (JV)	17EC71 (PSK)				
WED		17EC72 (JV)	17EC75X		17EC71 (PSK)	17EC73 (CDJ)				
THU		17EC73 (CDJ)	17EC71 (PSK)		17EC74X	17EC72 (JV)		17ECL76 (VMP+KB)-C1		
								17ECL77 (PSK+JV)-C2		
FRI		17EC75X	17EC73 (CDJ)		17ECL76 (VMP+RK)-C2					
					17ECL77 (PSK+BHS)-C1					
SAT										

Subject Code	Subject Name	Faculty Name
17EC71	Microwave and Antennas	Mr. Praveena K S (PSK)
17EC72	Digital Image Processing	Mr. Jashwanth V (JV)
17EC73	Power Electronics	Ms. Chaithanya D J (CDJ)
17EC741	Multimedia Communication	Mr. Yashwanth J (YJ)
17EC742	Biomedical Signal Processing	Dr. T P Surekha (TPS)
17EC744	Cryptography	Mr. Vishwas K Singh (VKS)
17EC745	CAD for VLSI	Dr. Geethashree A (GA)
17EC752	IOT and Wireless Sensor Networks	Dr. Vasudha M P (VMP)
17EC755	Satellite Communication	Mrs. Kavyashree B (KB), Ms. Ramya B (RB)
17ECL76	Advanced Communication Lab	
17ECL77	VLSI Lab	
17ECP78	Project Work Phase-I + Project Work Seminar	